2521/203 2602/202
2601/202 2603/202
DIGITAL AND ANALOGUE
ELECTRONICS II
Oct./Nov. 2022
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN ELECTRICAL AND ELECTRONICS ENGINEERING
(POWER OPTION)
(TELECOMMUNICATION OPTION)
(INSTRUMENTATION OPTION)

MODULE II

DIGITAL AND ANALOGUE ELECTRONICS II

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Answer booklet;
Mathematical tables/non-programmable scientific calculator;
*This paper consists of **EIGHT** questions in **TWO** sections, **A** and **B**.*
*Answer any **TWO** questions from section **A**, and any **THREE** questions from section **B** in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as indicated.
Candidates should answer the questions in English.

This paper consists of 6 printed pages and one insert.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

SECTION A: ANALOGUE ELECTRONICS II

*Answer any **TWO** questions from this section.*

1. (a) (i) State any **two** areas of application of liquid crystal displays (LCDs).

(ii) Differentiate the operating principles of the following types of LCDs when energised:

(I) field effect display;

(II) dynamic scattering.

(6 marks)

(b) With the aid of a diagram, explain the construction of a light emitting diode (LED).

(5 marks)

(c) (i) Explain how the Zener diode maintains a constant output voltage despite the variations in input voltage.

(ii) **Figure 1** shows a circuit diagram of a Zener shunt regulator. The Zener diode used in the circuit has a breakdown voltage of 5.1 V, a Zener resistance r_z of 10 Ω and the minimum and maximum values of Zener currents are 1 mA and 15 mA respectively. Determine the minimum and maximum values of the input voltage which can be regulated. (9 marks)

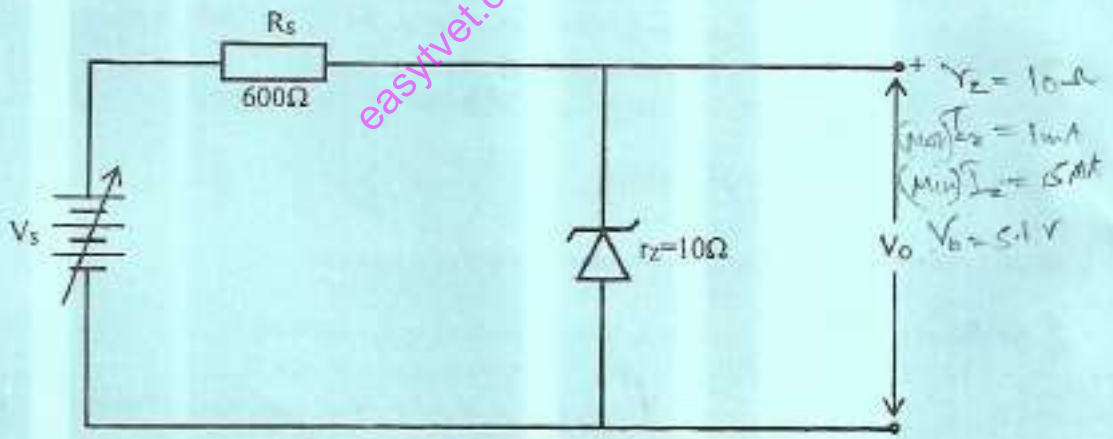


Fig. 1

2. (a) State **two**:

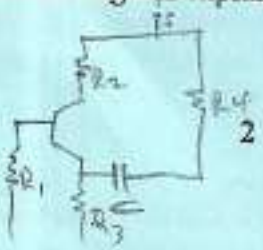
(i) ways of connecting feedback amplifiers;

(ii) merits of negative feedback connection.

(4 marks)

(b) With the aid of a circuit diagram explain the operation of an RC-phase shift oscillator circuit.

(8 marks)



(c) (i) A FET phase shift oscillator uses three identical RC sections in the feedback network. The values of the components are $R = 100\,k\Omega$ and $C = 0.01\,\mu F$. Determine the frequency of oscillations.

(ii) A Hartley oscillator is designed with $L_1 = 2\,mH, L_2 = 20\,\mu H$. Determine the value of capacitance if the frequency of oscillation is 2 MHz.

(iii) State **two** applications of oscillators.

(8 marks)

3. (a) (i) State **two** characteristics of an ideal OP-Amp.

(ii) Using a circuit diagram, show that the gain of an inverting amplifier is given by the expression:

$$A_v = \frac{-R_2}{R_1}$$

(7 marks)

(b) **Figure 2** shows an OP-Amp based summer. Determine the value of output voltage.

(3 marks)

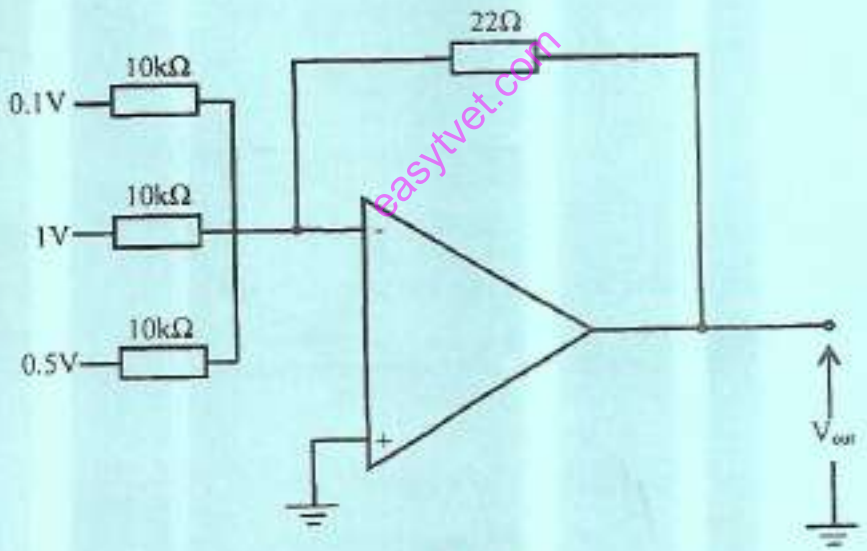


Fig. 2

(c) A transistor used in CB circuit has the following set of parameters: $h_{ib} = 36\,\Omega, h_{fb} = -0.98, h_{rb} = 5 \times 10^{-4}, h_{ob} = 10^{-6}$ siemens. With $R_s = 2\,k\Omega$ and $R_c = 10\,k\Omega$. Calculate:

(i) $\gamma_{in(base)}$;
(ii) γ_{out};
(iii) A_i;
(iv) A_v.

(10 marks)

SECTION B: DIGITAL ELECTRONICS

*Answer any **THREE** questions from this section.*

4. (a) State **two** methods of error detection. (2 marks)

(b) (i) State **two** advantages of using complement method of substraction.

(ii) (I) Using 2's complement, solve $17_{10} - 26_{10}$.

(II) Using 1's complement, perform the arithmetic $1F_{16} - B_{16}$. (9 marks)

(c) Using logic diagrams, illustrate how NOR gates can be used to generate the following functions:

(i) NOT operation;
(ii) AND operation;
(iii) OR operation. (9 marks)

5. (a) Perform each of the following:

(i) convert $26A_{16}$ to binary;

(ii) multiply 101.01_2 by 11.1_2;

(iii) convert binary number 11011011 to its Gray code equivalent.

(iv) add 8_{10} to 6_{10} in Excess 3 code and express the answer in Excess 3 code. (9 marks)

(b) **Figure 3** shows a logic circuit diagram of a logical network. Obtain the minimized expression of the output F. (4 marks)

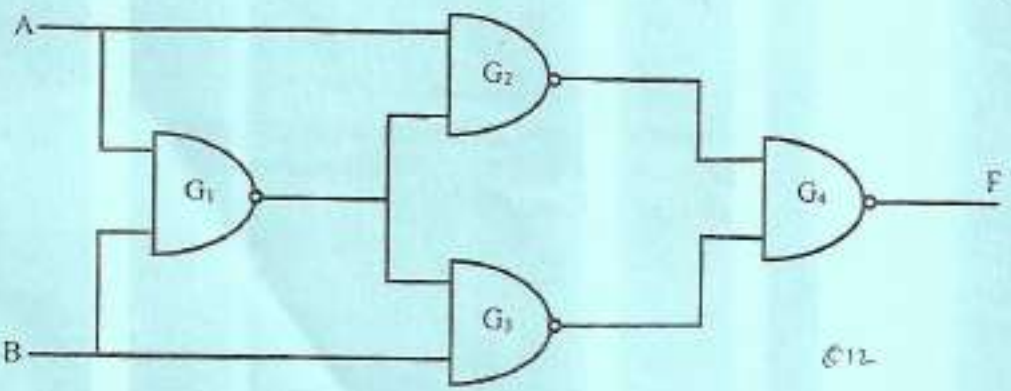


Fig. 3

(c) (i) Using Boolean rules, simplify the expression $F=(A+B)(B+C)$.

(ii) Draw the logic circuit diagram for the simplified expression in c (i).

(7 marks)

6. (a) Table 1 shows the classification of logic families.

Table 1

Category	No. of equivalent basic logic gates on a single chip
1	12 - 99
2	100 - 999
2	10,000 and above

Name the corresponding category of the logic families. (3 marks)

(b) With the aid of NAND gate based circuit diagram, explain the operation of an edge triggered J - K flip flop. (7 marks)

(c) (i) State any two performance characteristics of ECL gates.

(ii) With the aid of a circuit diagram, explain why a TTL gate with a totem pole output should not be wire ANDed.

(iii) State and explain a remedy to the situation in c (ii).

(10 marks)

7. (a) (i) Define each of the following with respect to digital - to analogue converters:

(I) resolution;
(II) speed.

(ii) A 6 bit analogue to digital converter has a maximum precision supply voltage of 20 V. Determine the:

(I) percentage resolution of the converter;
(II) analogue voltage represented by the least significant bit;
(III) analogue voltage equivalent to a digital output of 100110.

(8 marks)

(b) (i) Draw the truth table of a binary half adder circuit.

(ii) Obtain the Boolean expression for the outputs of the adder in b (i).

(iii) Implement the expressions in b (ii) using logic gates.

(6 marks)

(c) (i) State **two** advantages of MOSFET RAMs over BIPOLAR RAM memories.

(ii) Explain how an EPROM is erased and reprogrammed.

(6 marks)

8. (a) State any **three** applications of shift registers. (3 marks)

(b) With the aid of waveforms, explain the following terms as used in edge triggered flip flops:

(i) propagation delay (tpd);
(ii) set up time (ts);
(iii) hold time (tn).

(6 marks)

(c) State the operational difference between synchronous and asynchronous counters.

(2 marks)

(d) With the aid of truth table, logic circuit diagram and waveforms illustrate the operation of a 3 - bit negative edge clocked ripple counter. (9 marks)

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