2521/203, 2602/202
2601/202, 2603/202
**DIGITAL AND ANALOGUE
ELECTRONICS II**
June/July 2019
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING
(POWER OPTION)
(TELECOMMUNICATION OPTION)
(INSTRUMENTATION OPTION)
MODULE II

DIGITAL AND ANALOGUE ELECTRONICS II

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
   Answer booklet;
   Mathematical table/Non-programmable scientific calculator.
*The paper consists of **EIGHT** questions in **TWO** sections; A and B.*
*Answer any **TWO** questions from section A and any **THREE** questions from
section B in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as indicated.
Candidates should answer the questions in English.

This paper consists of 7 printed pages.

Candidates should check the question paper to ascertain that
all the pages are printed as indicated and that no questions are missing.

Turn over

SECTION A: ANALOGUE ELECTRONICS II

*Answer **TWO** questions from this section.*

1. (a)   With the aid of a diagram, explain the operation of a solid-state LASER.   (6 marks)

    (b)   Figure 1 shows a circuit diagram of a d.c over-voltage indicator using a unijunction
          transistor (UJT). Explain the operation of the circuit.   (4 marks)
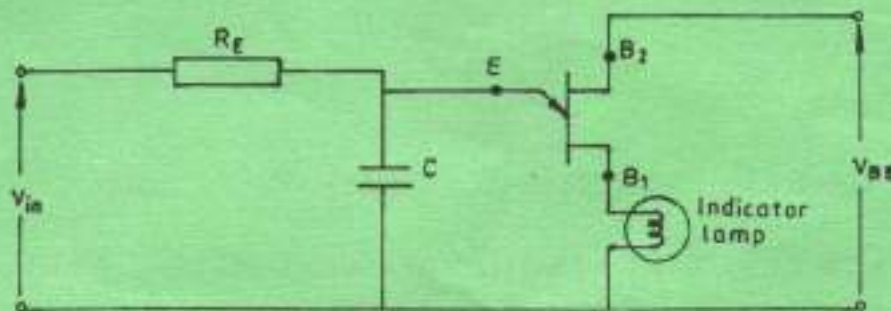

Fig. 1

    (c)   Figure 2 shows a circuit diagram of a transistor amplifier in common emitter
          configuration. The h-parameters of the transistor are:
          hie = 1500 Ω, hfe = 50; hre = 4 x 10^{-4}; hoe = 5 x 10^{-5} S

Fig. 2

Determine the:

    (i)   a.c load resistance, r_L;
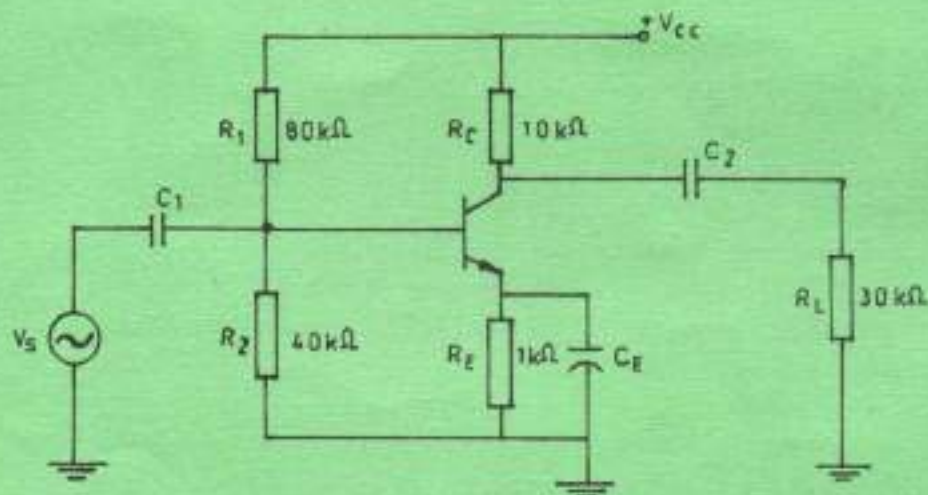   (ii)   a.c input impedance of the circuit;
    (iii)   voltage gain;
    (iv)   output impedance of the circuit.

                                                                    (10 marks)

2. (a) (i) State **three** characteristics of an ideal operational amplifier.

(ii) Figure 3 shows an op-amp based circuit diagram. The slew rate of the op-Amp is 0.5 v/μS. Determine the:

(I) closed loop voltage gain;

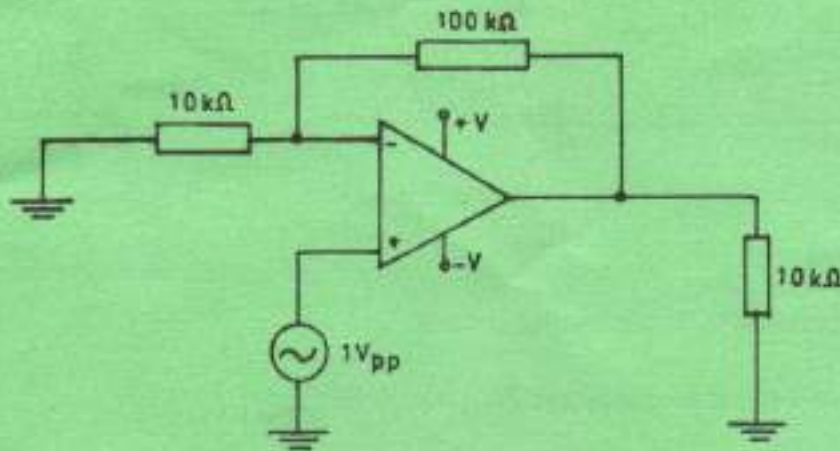(II) peak output voltage;

(III) maximum operating frequency.

(9 marks)

Fig 3

(b) A colpilts oscillator has a tank circuit consisting of two capacitors $C_1 = 0.001 \mu F$, $C_2 = 0.1 \mu F$ and an inductor L = 15 μH.

Determine the:

(i) effective capacitance;

(ii) operating frequency;

(iii) feedback fraction.

(6 marks)

(c)   Figure 4 shows a circuit diagram of a blocking oscillator. Explain its operation.
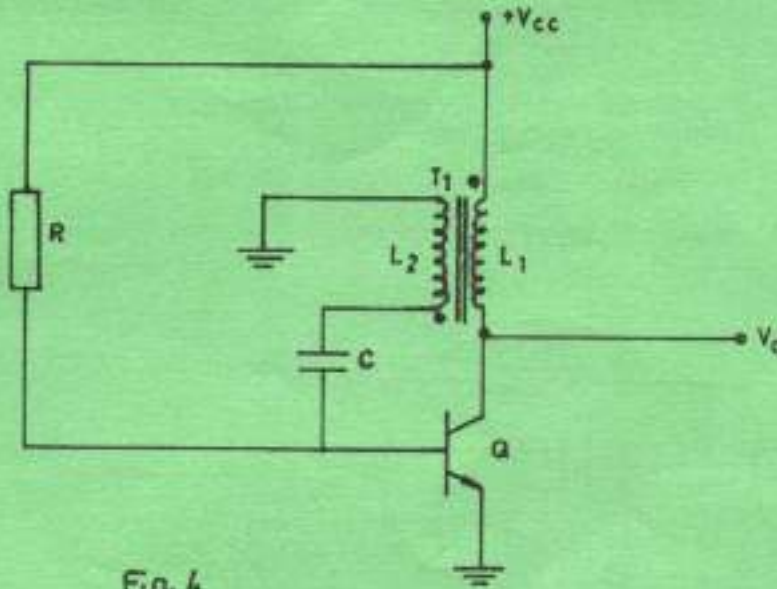
(5 marks)

Fig. 4

3. (a)   State **three** applications of integrating circuits.   (3 marks)

(b)   Figure 5 shows a tuned amplifier circuit. Determine:

(i)   the resonant frequency;

(ii)   the Q of the tank circuit;
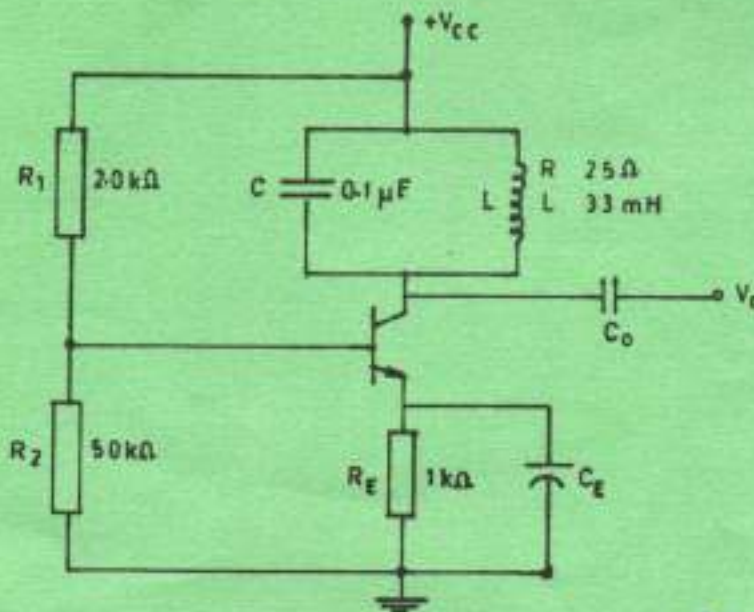
(iii) bandwidth of the amplifier.

(8 marks)

Fig. 5

(c) (i) State **three** merits of negative feedback.

(ii) An amplifier has an open loop gain of $A = 100$, input resistance, $R_i = 100\ \Omega$, output resistance $R_o = 1000\ \Omega$. The amplifier is connected with negative feedback in shunt-series topology. The feedback factor $\beta = 0.1$. Determine:

(I) closed loop gain;

(II) input resistance with feedback;

(III) output resistance with feedback.

(9 marks)

SECTION B: DIGITAL ELECTRONICS

*Answer **THREE** questions from this section.*

4. (a) Perform the following number conversions:

(i) 25.5_{10} to binary;

(ii) 2220_{10} to hexadecimal;

(iii) $9B2.1A_H$ to decimal;

(iv) 262_{10} to octal.

(9 marks)

(b) Perform the following operations:

(i) $101101_2 \div 101_2$;

(ii) $11001_2 + (-10110_2)$ using 1's complement;

(iii) $65_{10} + 58_{10}$ in BCD.

(11 marks)

5. (a) Draw the truth table of a 2-input X-NOR gate. (2 marks)

(b) A boolean expression is given by:

$$F = \overline{A}BC + ABC + B\overline{C}D$$

(i) Obtain a truth table for the expression;

(ii) Simplify the expression using a Karnaugh map;

(iii) Realize the function using NAND gates only

(12 marks)

(c)   Figure 6 shows a logic circuit diagram.

   (i)   Derive the expression for the output Z;

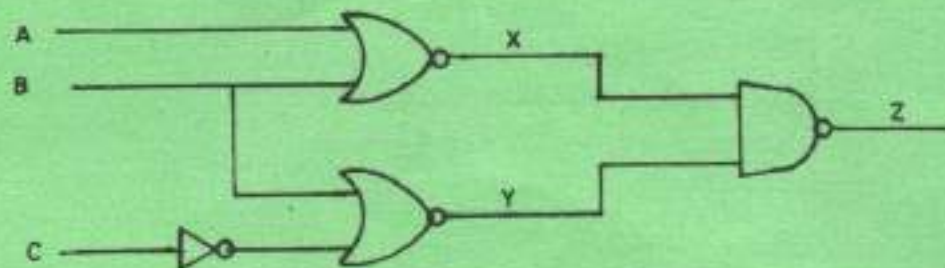   (ii)   Using the De Morgan's theorem, obtain a simplified expression for the output Z.

   (6 marks)

Fig. 6

6.   (a)   (i)   State **three** areas of application of digital to analogue converters (ADCs).

      (ii)   A 5-bit successive approximation analogue to digital converter uses a 2 MHz clock and 8V reference. Determine:

      (I)   conversion time;
      (II)   resolution in volts.

      (7 marks)

   (b)   Contrast between serial– and parallel– adders.   (4 marks)

   (c)   (i)   Draw the truth table of a 4:1 multiplexer.

      (ii)   Obtain the boolean expression for the multiplexer in c(i).

      (iii)   Implement the expression in c(ii) using logic gates.

      (9 marks)

7.   (a)   With the aid of a diagram, explain the operation of a 4-bit binary parallel-in parallel-out (PIPO) shift register using D-type flip flops.   (7 marks)

   (b)   (i)   State **two** limitations of ripple counter.

      (ii)   Draw a logic circuit diagram of a mod-8 ripple counter using JK flip flops and describe its operation.

      (8 marks)

   (c)   (i)   Define each of the following with respect to logic families:

      (I)   Fan-out;
      (II)   Noise margin.

    (ii)   State **three** precautions to be observed when using TTL devices in digital circuits.

                      (5 marks)

8.   (a)   Define each of the following with respect to memories:

            (i)   volatile;
            (ii)   access time.

                      (2 marks)
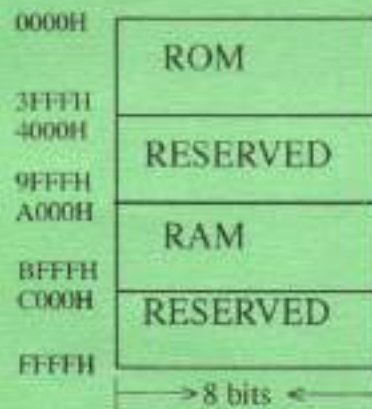
    (b)   Figure 7 shows a microcomputer memory map.

            (i)   Determine the amount of memory in kilobytes dedicated to:

                  (I)   RAM;
                  (II)   ROM.

            (ii)   Determine the number of address lines required to address:

                  (I)   RAM;
                  (II)   ROM.

                      (8 marks)

```
0000H  ┌──────────────┐
       │     ROM      │
3FFFH  │              │
4000H  ├──────────────┤
       │   RESERVED   │
9FFFH  │              │
A000H  ├──────────────┤
       │     RAM      │
BFFFH  │              │
C000H  ├──────────────┤
       │   RESERVED   │
FFFFH  └──────────────┘
       |── 8 bits ──|
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    (c)   With the aid of a diagram, describe the operation of a dynamic RAM (D-RAM) MOS cell.   (6 marks)

    (d)   State **two**:

            (i)   merits of dynamic-RAM (D-RAM);
            (ii)   demerits of static RAM (S-RAM).

                      (4 marks)

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