## SECTION A: ANALOGUE ELECTRONICS II

*Answer any **TWO** questions from this section.*

1. (a) (i) State **two** advantages of a silicon controlled switch (SCS) over a silicon controlled rectifier (SCR).

(ii) Figure 1 shows a circuit diagram of an alarm system employing a silicon controlled switch. Describe its operation.

(6 marks)

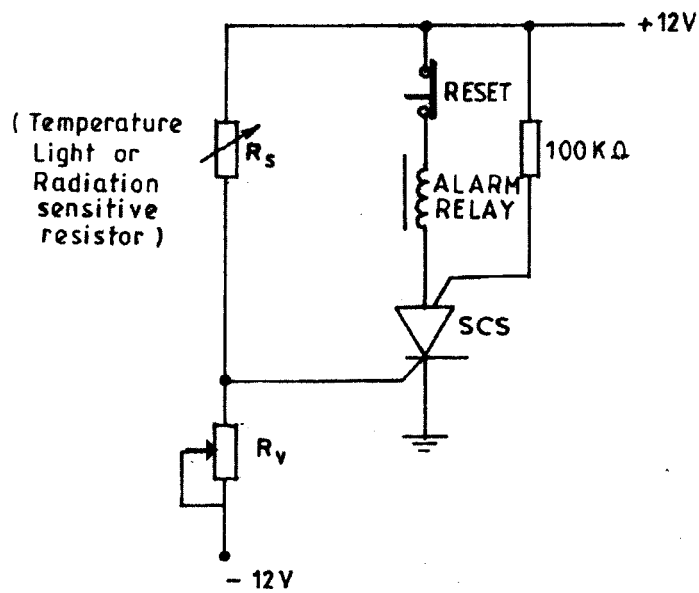



Fig. 1

(b) With the aid of a circuit diagram, describe the operation of a discrete-component bistable multivibrator. (8 marks)

(c) An LED has the following ratings: power output $P_0 = 0.42$ mW, forward current $I_F = 80$ mA and forward voltage $V_F = 1.22$V. It is connected in series with a current limiting resistor and supplied from a 5V source. The light from the LED is projected onto a flat surface 2.54 cm away and forms a divergence angle of 0.524 radians. Determine the:

(i) value of the current limiting resistor;
(ii) area illuminated by the LED;
(iii) incident irradiance at the flat surface.

(6 marks)

2. (a) (i) State the **two** conditions necessary for oscillations to be sustained in a sinusoidal oscillator.

(ii) With the aid of a circuit diagram, describe the operation of a blocking oscillator.

(10 marks)

(b) An amplifier has a gain A = 100, input resistance $Ri = 2K\Omega$ and output resistance $Ro = 40\ K\Omega$. Determine the following when it is connected as a voltage-series negative feedback amplifier with a feedback factor $\beta = 1/10$:

(i) gain;
(ii) input resistance;
(iii) output resistance;
(iv) reduction in distortion;
(v) percentage change in gain with feedback if the gain without feedback changes by 20%.

(10 marks)

3. (a) (i) Define the following with respect to operational amplifiers:

(I) input offset voltage;
(II) slew rate;
(III) common-mode voltage gain.

(ii) Figure 2 shows a circuit diagram of a first-order low-pass filter. Determine the:

(I) voltage gain;
(II) cutoff frequency.

(7 marks)

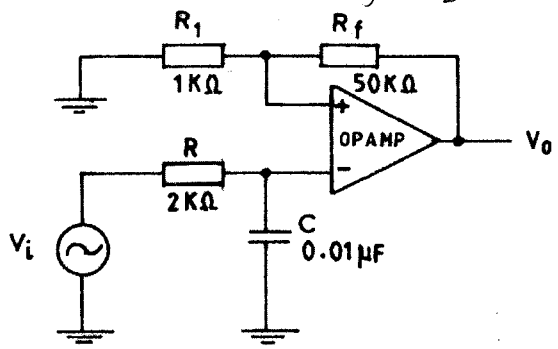



Fig. 2

(b) Table 1 shows the data of the gain/frequency characteristic of a two-stage tuned radio frequency amplifier.

(i) Plot, on the same axis, the gain/frequency curves for:

(I) single stage;
(II) two stages.

(ii) From the curves, determine the bandwidth of the single stage and the two stages.

(7 marks)

Table 1

| Frequency | 950 | 960 | 970 | 980 | 990 | 1000 | 1010 | 1020 | 1030 | 1040 | 1050 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Gain of 1 stage | 1.98 | 2.45 | 3.12 | 4.47 | 7.07 | 10 | 7.07 | 4.47 | 3.12 | 2.45 | 1.98 |
| Gain of 2 stages | 3.92 | 5.91 | 9.73 | 19.98 | 50 | 100 | 50 | 19.98 | 9.73 | 5.91 | 3.92 |

(c) Show that the maximum theoretical efficiency of a class-B power amplifier is 78.54%. (6 marks)

## SECTION B: DIGITAL ELECTRONICS

*Answer any **THREE** questions from this section.*

4. (a) Perform the following number system conversion:

(i) $1011101001_2$ to decimal;

(ii) $EB4A_{16}$ to decimal (6 marks)

(b) Perform the following arithmetic operations in the given bases:

(i) $1011_2 \times 101_2$

(ii) $1A8_{16} + 67B_{16}$ (6 marks)

(c) (i) Table 2 shows the ASC11 code for alphanumeric characters. Obtain the:

(I) code for the letter *e*;

(II) decimal number represented by the code 0111001.

Table 2

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 0 | NUL | DLE | SP | 0 | @ | P | ` | p |
| 1 | SOH | DC1 | ! | 1 | A | Q | a | q |
| 2 | STX | DC2 | " | 2 | B | R | b | r |
| 3 | ETX | DC3 | # | 3 | C | S | c | s |
| 4 | EOT | DC4 | $ | 4 | D | T | d | t |
| 5 | ENQ | NAK | % | 5 | E | U | e | u |
| 6 | ACK | SYN | & | 6 | F | V | f | v |
| 7 | BEL | ETB | ' | 7 | G | W | g | w |
| 8 | BS | CAN | ( | 8 | H | X | h | x |
| 9 | HT | EM | ) | 9 | I | Y | i | y |
| A | LF | SUB | • | : | J | Z | j | z |
| B | VT | ESC | + | ; | K | [ | k | { |
| C | FF | FS | ' | < | L | \ | l | ¦ |
| D | CR | GS | - | = | M | ] | m | } |
| E | SO | RS | . | > | N | ^ | n | ~ |
| F | SI | US | / | ? | O | - | o | DEL |

0110 0100 0111
0100 1001 0010
1010 1101 1010

(ii) Add $647_{10}$ to $492_{10}$ in the 8421 BCD code.

(8 marks)

5. (a) (i) Define the following with respect to edge-triggered flip-flops:

(I) set-up time; this is the time when a flipflop is meant to operate
(II) hold-up time. - is the time when a flipflop is meant to wait before acting

(ii) With the aid of a logic diagram, describe the operation of a master-slave JK flip-flop when the clock is at logic 1 and makes a transition to logic 0. Assume the circuit is initially reset and the inputs J = K = 1.

(9 marks)

(b) (i) State **two** applications of binary counters.

in arithmetic
in multiplexer & statistic
store data

(ii) Figure 3 shows a logic diagram of a binary counter. Describe its operation for three clock pulses and draw the timing diagrams.

(8 marks)

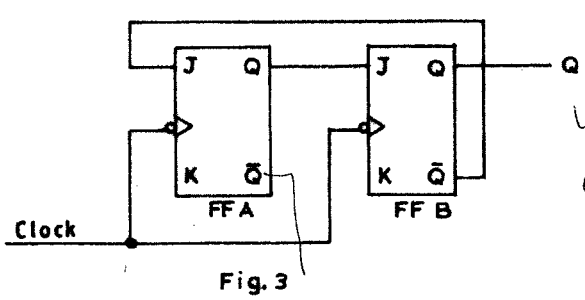



Fig. 3

When clock is trigger the
CLK

(c) Draw the state diagram of a 4-bit Johnsons counter assuming that all the stages are in the '0' state. (3 marks)

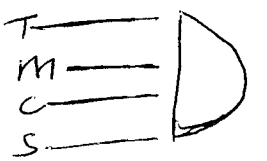
6. (a) Using Boolean algebra, simplify the equation

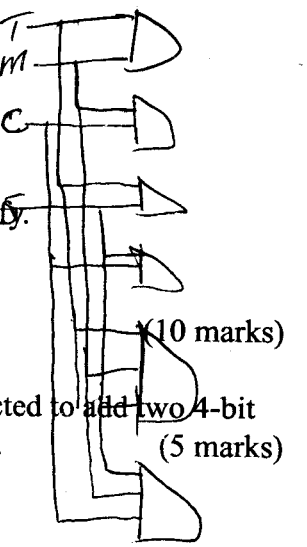
$$F = \overline{A}\,(B + \overline{C})(A + \overline{B} + C)\overline{(A\,B\,C)}$$

(5 marks)

(b) A digital vending machine is to dispense beverage at a time as indicated:

- Tea and milk
- Coffee and milk
- Tea and sugar
- Coffee and sugar
- Tea, milk and sugar
- Coffee, milk and sugar




(i) Draw the truth table for the vending machine operation.

(ii) Obtain the logic expression from the truth table and simplify.

(iii) Implement the simplified expression in b(ii).

(10 marks)

(c) Figure 4 shows a logic diagram of a serial adder/subtractor connected to add two 4-bit binary numbers. Outline the sequence of adding the two numbers.

(5 marks)

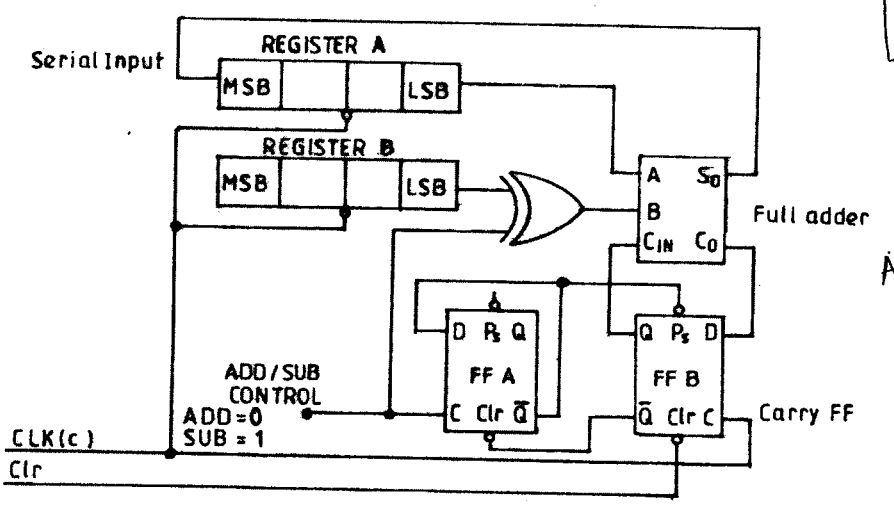



Fig. 4

7. (a) (i) Distinguish between random access memory (RAM) and read only memory (ROM).

(ii) With the aid of a circuit diagram, explain how a programmable ROM is programmed.

(8 marks)

(b) With the aid of a labelled block diagram, describe the operation of a ramp-type analog-to-digital converter.

(8 marks)

(c) Figure 5 shows a circuit diagram of a weighted resistor digital-to-analog converter. Determine the value of the output voltage, Vo. (4 marks)

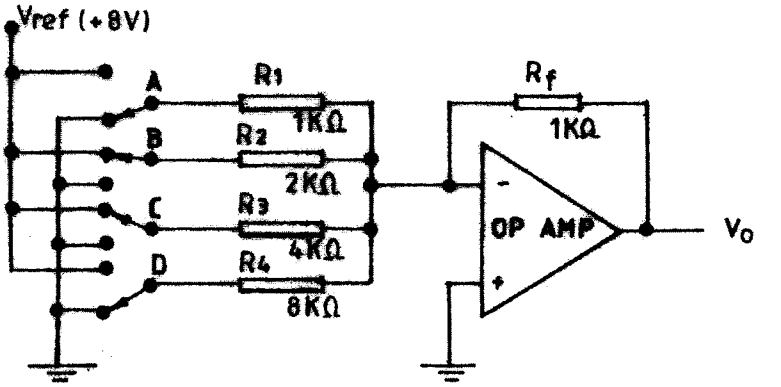



Fig. 5

8. (a) (i) State the packaging density of the following ICs:

(I) medium scale integration;
(II) very large scale integration.

(ii) With the aid of a circuit diagram, describe the operation of a two-input CMOS NOR gate.

(10 marks)

(b) Figure 6 shows a circuit diagram of a transistor switch. If $V_{be} = 0.6V$, $V_{ce(sat)} = 0.2V$ and $\beta = 50$; determine the value of the base resistance at which the transistor will saturate. (10 marks)

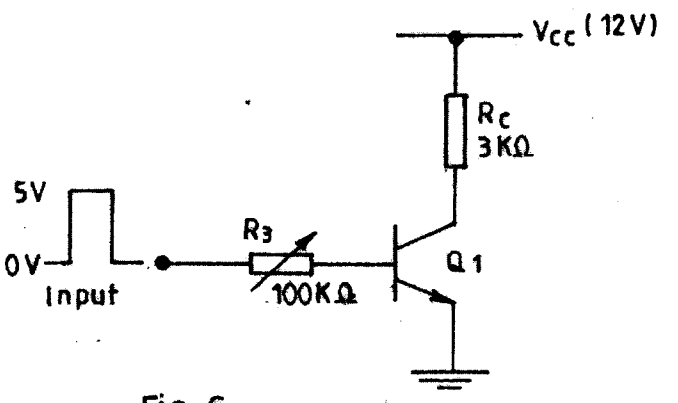



Fig. 6

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