SECTION A: MICROPROCESSOR SYSTEMS

*Answer any **THREE** questions from this section*

1. (a) With the aid of a diagram, explain the functions of the elements of a microcomputer. (6 marks)

(b) State the functions of the following microprocessor status register flags:

(i) carry flag (C);
(ii) zero flag (Z);
(iii) sign flag (S);
(iv) overflow flag (V). (4 marks)

(c) Distinguish between byte and word as applied to microprocessors. (2 marks)

(d) (i) Describe the process of erasing and programming an EPROM. (4 marks)
(ii) Explain the functions of the following software development tools:

(I) Debugger;
(II) Assembler. (4 marks)

2. (a) Describe Direct Memory Access (DMA) data transfer process in microprocessor-based systems. (5 marks)

(b) Figure 1 shows an Intel 8085 microprocessor pin configuration. State the pins that will execute the following:

(i) CPU control;
(ii) Data transfer controls;
(iii) Address transfer;
(iv) Data transfer. (6 marks)

Fig. 1

(c) Describe the following fault finding equipment in microprocessors:

(i) logic analyzer;
(ii) signature analyzer;
(iii) cathode ray oscilloscope. (9 marks)

3. (a) With the aid of a timing diagram, explain the fetch-decode-execute cycle. (8 marks)

(b) Describe **three** functions of microcomputer operating system. (6 marks)

(c) Table 1 shows intel 8085 assembly language program segment, hand code the program into hexadecimal machine code.

Table 1

```
        ORG 1800 H
        LXIH, 0014 H
        MVI B, 03 H
BACK:   DADH
        DCR B
        JNZ BACK
        SHLD 5000 H
        HLT
```

(6 marks)

4. (a) (i) Define 'addressing mode' as applied to microprocessors. (1 mark)

(ii) Describe each of the following microprocessor addressing modes stating an example in each case:

(I) immediate addressing;
(II) direct addressing;
(III) register indirect addressing. (6 marks)

(b) With the aid of a diagram, explain the daisy chaining interrupt control of three input-output (I/O) devices. (8 marks)

(c) The Intel 8085 microprocessor has **five** levels of interrupts. List these levels in descending order of priority. (5 marks)

5. (a) (i) With the aid of a diagram, show how a microprocessor is interfaced with a Universal Asynchronous Receiver Transmitter (UART).

(ii) Explain how data is transmitted from a microcomputer through the interface in a (i). (6 marks)

(b) Write an assembly language program using a subroutine to multiply any 8-bit number by 7. (6 marks)

(c) With the aid of a flowchart, write a program to sum 8 bytes of data in memory location 2000 H - 2007 H and store the result in location 2020 H. (8 marks)

SECTION B: MICROCONTROLLER TECHNOLOGY

*Answer any **TWO** questions from this section*

6. (a) Define each of the following as used in process control:

(i) dead band;
(ii) process variable;
(iii) lag time. (3 marks)

(b) With the aid of a diagram, explain the construction and operation of a pneumatic actuator. (6 marks)

(c) A stepper motor has 4 electromagnetic coils, 8 poles and 6 teeth on the rotor. It is supplied by a 4 phase stator. Determine the:

(i) spacing of the poles in the motor in degrees;
(ii) steps for the rotor to complete one full revolution;
(iii) step angle. (6 marks)

(d) Figure 2 shows a PI pneumatic controller. Explain how it operates. (5 marks)

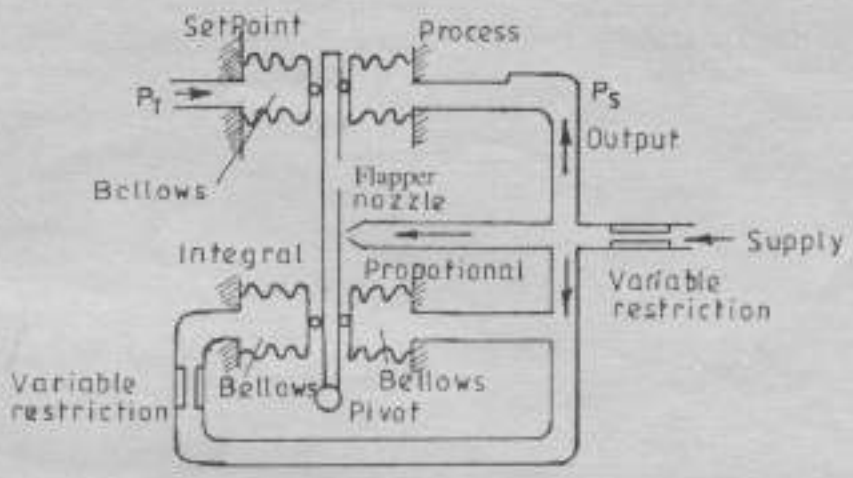

Fig. 2

7. (a) Describe the operation of a sequential control system. (3 marks)

(b) Describe each of the following components found in a SCADA network:

(i) data acquisition server;
(ii) human machine interface;
(iii) communication interface. (6 marks)

(c) (i) State **three** types of timers found in PLCs. (3 marks)

(ii) A program is used to carry out the sequential switching ON of three motors A, B and C. When the start switch is closed motor A starts, 10 seconds later, motor B starts and after 30 seconds motor C starts. Draw the ladder diagram for the control.

(iii) Explain the operation of the switching in C (ii). (8 marks)

8. (a) Describe the following types of robotic sensors, stating an example in each case:

(i) tactile;
(ii) proximity. (4 marks)

(b) (i) Describe an industrial robot.
(ii) Explain the working of the following parts of a robot:

(I) manipulator;
(II) end-effector;
(III) motors. (8 marks)

(c) A robot has been constructed to control three safes with lockable doors that have sensors mounted on them. Safe A has two doors that close to cause a third door on this safe to open whenever the robot touches them. Safe B has two doors that close when the robot touches them. A third door on this safe closes whenever the robot touches the two doors. The action of safe A or B causes third safe C to open its third door. Let opening be logic 1, closing be logic 0. Draw a:

(i) logic circuit to implement the actions of the three safes;
(ii) truth table to describe safes A, B and C individually.

(8 marks)

Outputs

Opening	Closing	A	B	C
		0	0	0
		0	1	
		1	0	
		1	1	

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	28	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LXI B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SP,D16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	–	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	90	SUB B	BB	CMP E	E6	ANI D8
10	–	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	–
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	XRI D8
18	–	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	–	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	–
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	–	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.

Appendix A: Instruction Set of 8051 Microcontroller

Mnemonics, Arranged Alphabetically

MNEMONIC	DESCRIPTION	BYTES	CYCLES	FLAGS
ACALL addr11	PC + 2 → (SP); addr11 → PC	2	2	
ADD A, direct	A + (direct) → A	2	1	C OV AC
ADD A, @Ri	A + (Ri) → A	1	1	C OV AC
ADD A, #data	A + #data → A	2	1	C OV AC
ADD A, Rn	A + Rn → A	1	1	C OV AC
ADDC A, direct	A + (direct) + C → A	2	1	C OV AC
ADDC A, @Ri	A + (Ri) + C → A	1	1	C OV AC
ADDC A, #data	A + #data + C → A	2	1	C OV AC
ADDC A, Rn	A + Rn + C → A	1	1	C OV AC
AJMP addr11	Addr11 → PC	2	2	
ANL A, direct	A AND (direct) → A	2	1	
ANL A, @Ri	A AND (Ri) → A	1	1	
ANL A, #data	A AND #data → A	2	1	
ANL A, Rn	A AND Rn → A	1	1	
ANL direct, A	(direct) AND A → (direct)	2	1	
ANL direct, #data	(direct) AND #data → (direct)	3	2	
ANL C, bit	C AND bit → C	2	2	C
ANL C, /bit	C AND $\overline{bit}$ → C	2	2	C
CJNE A, direct, rel	[A <> (direct)]: PC + 3 + rel → PC	3	2	C
CJNE A, #data, rel	[A <> data]: PC + 3 + rel → PC	3	2	C
CJNE @Ri, #data, rel	[(Ri) <> data]: PC + 3 + rel → PC	3	2	C
CJNE Rn, #data, rel	[Rn <> data]: PC + 3 + rel → PC	3	2	C
CLR A	0 → A	1	1	
CLR bit	0 → bit	2	1	
CLR C	0 → C	1	1	0
CPL A	$\overline{A}$ → A	1	1	
CPL bit	$\overline{bit}$ → bit	2	1	
CPL C	$\overline{C}$ → C	1	1	C
DA A	Abin → Adec	1	1	C
DEC A	A – 1 → A	1	1	
DEC direct	(direct) – 1 → (direct)	2	1	
DEC @Ri	(Ri) – 1 →(Ri)	1	1	
DEC Rn	Rn – 1 → Rn	1	1	
DIV AB	A/B → AB	1	4	0 OV
DJNZ direct, rel	[(direct) – 1 <> 00]: PC + 3 + rel → PC	3	2	
DJNZ Rn, rel	[Rn – 1 <> 00]: PC + 2 + rel → PC	2	2	
INC A	A + 1 → A	1	1	
INC direct	(direct) + 1 → (direct)	2	1	
INC DPTR	DPTR + 1 → DPTR	1	2	
INC @Ri	(Ri) + 1 → (Ri)	1	1	
INC Rn	Rn + 1 → Rn	1	1	
JB bit, rel	[b=1]: PC + 3 + rel → PC	3	2	
JBC bit, rel	[b=1]: PC + 3 + rel → PC; 0 → bit	3	2	
JC rel	[C= 1]: PC + 2 + rel → PC	2	2	
JMP @A + DPTR	DPTR + A → PC	1	2	
JNB bit, rel	[b=0]: PC + 3 + rel → PC	3	2	
JNC rel	[C=0]: PC + 2 + rel → PC	2	2	
JNZ rel	[A>00]: PC + 2 + rel → PC	2	2	
JZ rel	[A=00]: PC + 2 + rel → PC	2	2	
LCALL addr16	PC + 3 → (SP); addr16 → PC	3	2	
LJMP addr16	Addr16 → PC	3	2	
MOV A, direct	(direct) → A	2	1	
MOV A, @Ri	(Ri) → A	1	1	
MOV A, #data	#data → A	2	1	
MOV A, Rn	Rn → A	1	1	
MOV direct, A	A → (direct)	2	1	
MOV direct, direct	(direct) → (direct)	3	2	
MOV direct, @Ri	(Ri) → (direct)	2	2	
MOV direct, #data	#data → (direct)	3	2	
MOV direct, Rn	Rn → (direct)	2	2	
MOV bit, C	C → bit	2	2	C
MOV C, bit	bit → C	2	1	
MOV @Ri, A	A → (Ri)	1	1	
MOV @Ri, direct	(direct) → (Ri)	2	2	

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